an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy within a contact opening in the insulating layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

61. (New) The memory device of claim 60, wherein the titanium alloy includes titanium and zinc.

62. (New) The memory device of claim 60, wherein the insulator layer includes silicon dioxide (SiO_2).

63. (New) The memory device of claim 60, wherein the electronic device includes a transistor.

64. (New) A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

a transistor formed on the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy within a contact opening in the insulating layer, the contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group

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consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

65. (New) The memory device of claim 64, wherein the titanium alloy includes titanium and zinc.

66. (New) The memory device of claim 64, wherein the insulator layer includes silicon dioxide (SiO_2).

67. (New) The memory device of claim 64, wherein the contact opening includes a high aspect ratio contact opening.

68. (New) A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

an electronic device formed on the semiconductor substrate, the electronic device having an active region;

a borophosphous silicate glass (BPSG) layer over the active region;

an alloy layer of a titanium alloy within a contact opening in the borophosphous silicate glass (BPSG) layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

69. (New) The memory device of claim 68, wherein the titanium alloy includes titanium and zinc.

70. (New) The memory device of claim 68, wherein the electronic device includes a transistor.

71. (New) The memory device of claim 68, wherein the contact opening includes a high aspect ratio contact opening.

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72. (New) A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

73. (New) The memory device of claim 72, wherein the titanium alloy includes titanium and zinc.

74. (New) The memory device of claim 72, wherein the electronic device includes a transistor.

75. (New) The memory device of claim 72, wherein the insulator layer includes silicon dioxide (SiO_2).

76. (New) The memory device of claim 72, wherein the insulator layer includes borophosphous silicate glass (BPSG).

77. (New) A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

78. (New) The memory device of claim 77, wherein the titanium alloy includes titanium and zinc.

79. (New) The memory device of claim 77, wherein the insulator layer includes silicon dioxide (SiO_2).

80. (New) The memory device of claim 77, wherein the insulator layer includes borophosphous silicate glass (BPSG).

81. (New) A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

a borophosphous silicate glass (BPSG) layer over the source/drain region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the borophosphous silicate glass (BPSG) layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

82. (New) The memory device of claim 81, wherein the titanium alloy includes titanium and zinc.